100

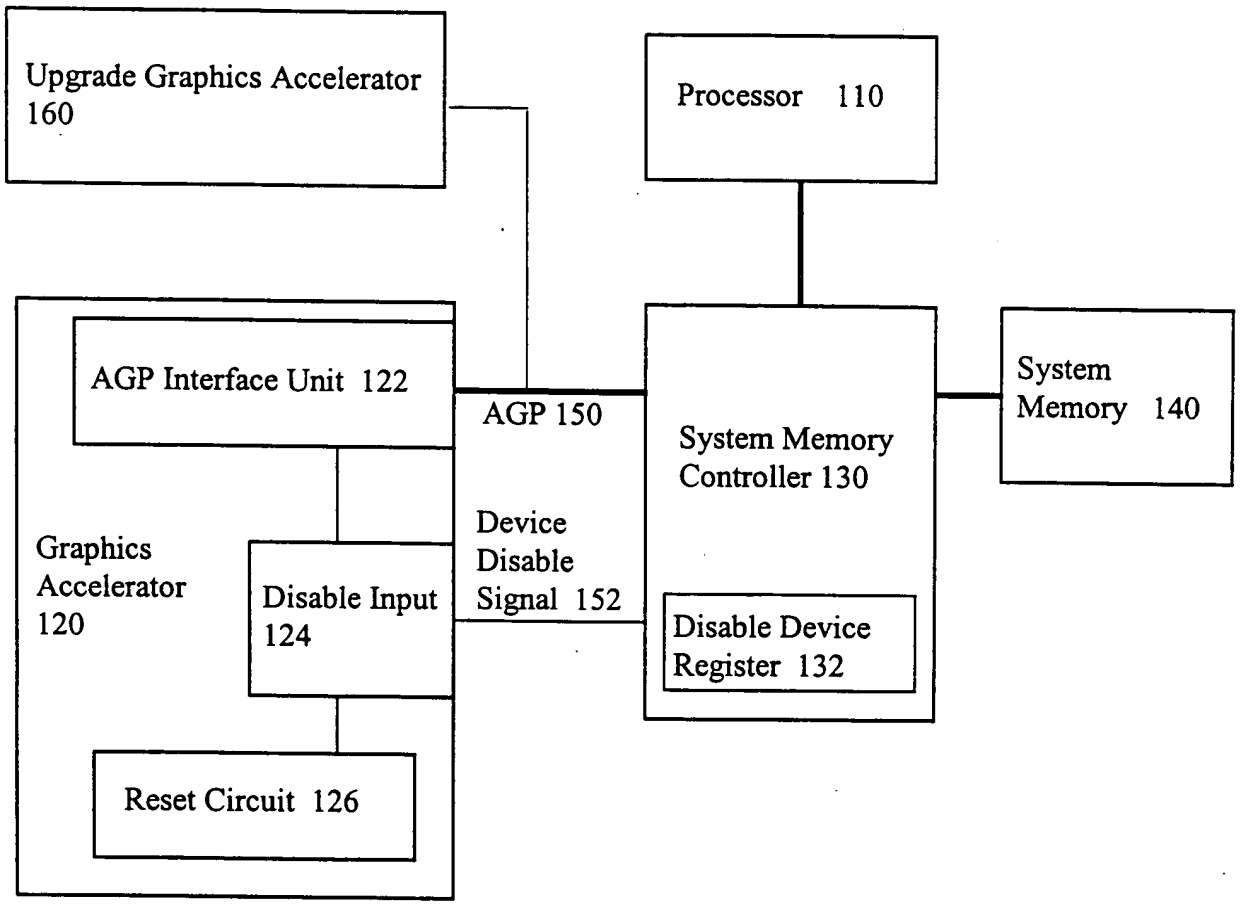

Upgrade Graphics Accelerator 160
Processor 110
AGP Interface Unit 122
AGP 150
System Memory Controller 130
System Memory 140
Graphics Accelerator 120
Disable Input 124
Device Disable Signal 152
Disable Device Register 132
Reset Circuit 126

Figure 1

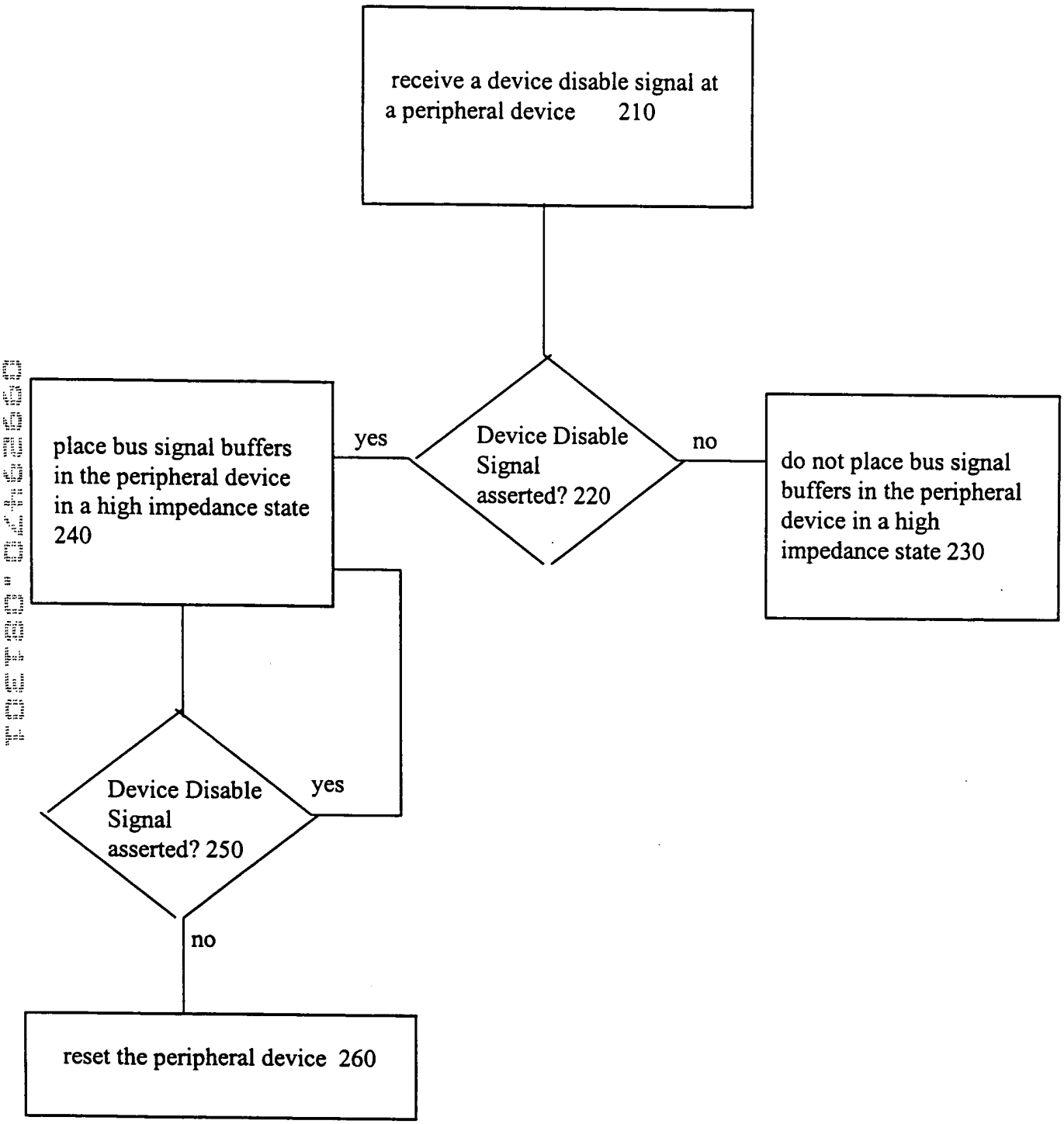
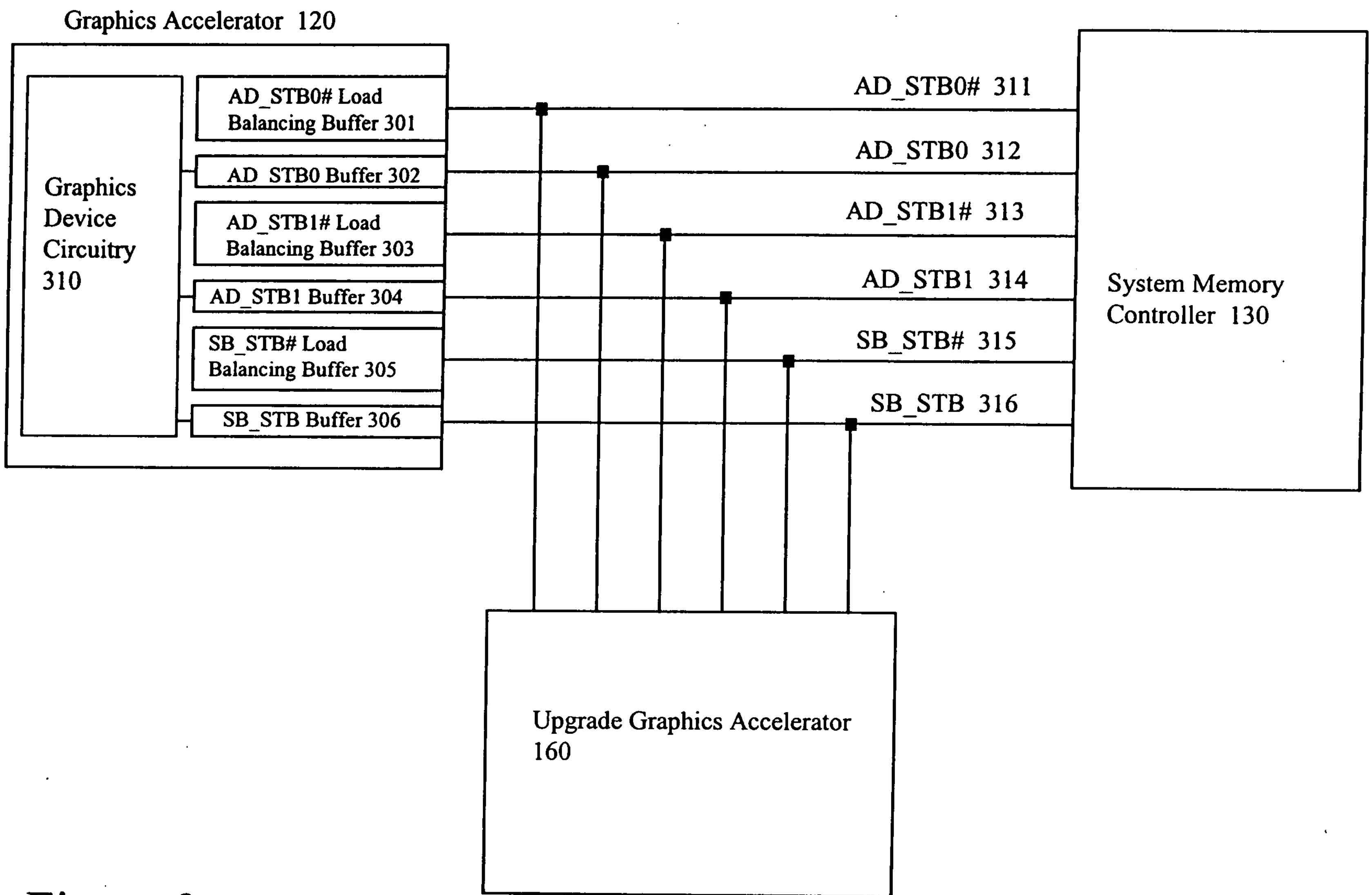

receive a device disable signal at a peripheral device 210
Device Disable Signal asserted? 220
yes
no
place bus signal buffers in the peripheral device in a high impedance state 240
do not place bus signal buffers in the peripheral device in a high impedance state 230
Device Disable Signal asserted? 250
yes
no
reset the peripheral device 260

Figure 2



Graphics Accelerator 120
Graphics Device Circuitry 310
AD_STB0# Load Balancing Buffer 301
AD_STB0 Buffer 302
AD_STB1# Load Balancing Buffer 303
AD_STB1 Buffer 304
SB_STB# Load Balancing Buffer 305
SB_STB Buffer 306
AD_STB0# 311
AD_STB0 312
AD_STB1# 313
AD_STB1 314
SB_STB# 315
SB_STB 316
System Memory Controller 130
Upgrade Graphics Accelerator 160

Figure 3

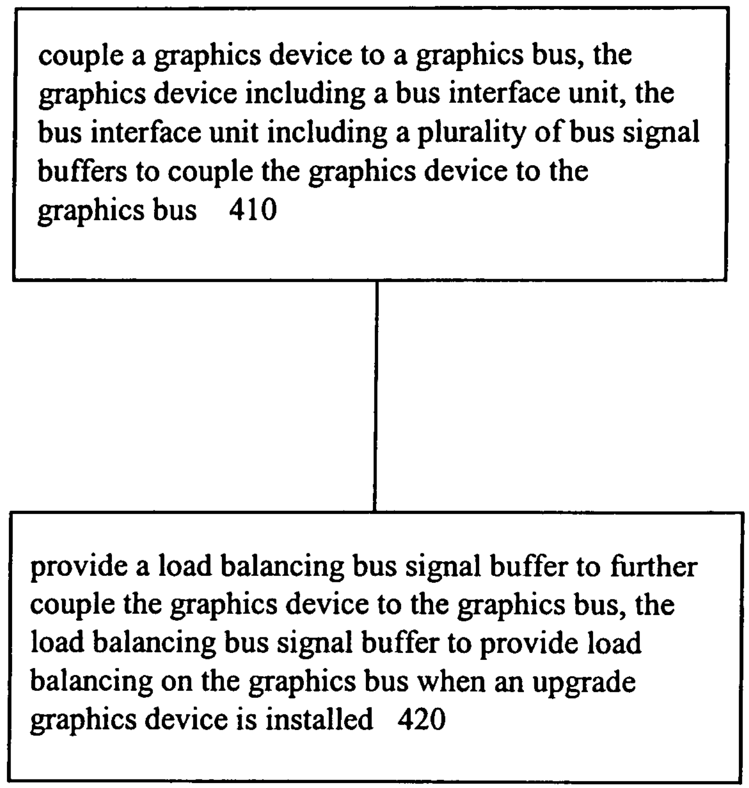

couple a graphics device to a graphics bus, the graphics device including a bus interface unit, the bus interface unit including a plurality of bus signal buffers to couple the graphics device to the graphics bus 410
provide a load balancing bus signal buffer to further couple the graphics device to the graphics bus, the load balancing bus signal buffer to provide load balancing on the graphics bus when an upgrade graphics device is installed 420

Figure 4